

WHAT IS CLAIMED IS:

1. A communication device comprising:
 - a physical layer device having:
 - a media driver connectable to a transmission medium;
 - a media receiver connectable to the transmission medium; and
 - a serializer/deserializer (serdes) connected to the media driver and the media receiver;
 - a master circuit connected to the serdes, the master circuit having:
 - a first physical layer data driver, the first physical layer data driver driving a millivolt differential signal; and
 - a first physical layer data receiver; and
 - a processing circuit having:
 - an internal circuit; and
 - a slave circuit connected to the internal circuit and the master circuit, the slave circuit having:
 - a first processing data receiver connected to the first physical layer data driver, the first processing data receiver outputting a first signal in response to receiving the signal output from the first physical layer data driver; and
 - a first processing data driver connected to the first physical layer data receiver, and connectable to the first processing data receiver.

2. The device of claim 1

- 25 wherein the master circuit further includes a clock driver connected to the serdes, the clock driver driving a millivolt differential signal;

wherein the slave circuit further includes a clock receiver connected to the clock driver, the clock receiver outputting a clock signal in response to a signal received from the clock driver; and
5 wherein the first processing data driver is connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver, the first physical layer data receiver receiving the clock signal when the first processing data driver is connected to receive the clock signal, and the first signal when the first processing data driver is connected to receive the first signal.
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3. The device of claim 2 wherein the master circuit further comprises an aligner connected to the first physical layer data receiver, the aligner receiving the clock signal when the first physical layer data receiver receives the clock signal, the aligner receiving the first signal when the first physical layer data receiver receives the first signal, the aligner having phase comparison circuitry that compares a phase of the clock signal received by the aligner with a phase of the first signal received by the aligner to determine a phase difference.
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20 4. The device of claim 3 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signals to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the signal output from the first physical layer data driver so that the first signal received by the aligner is substantially in phase with the clock signal received by the aligner.
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5. The device of claim 4 wherein the slave circuit further includes:

5 a first multiplexor connected to the clock input receiver and the first processing data receiver, the first multiplexor passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

10 a second multiplexor connected to the first multiplexor and the first communication data driver, the second multiplexor passing a signal output from the first multiplexor when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexor being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

15 6. The device of claim 5 wherein the slave circuit further includes a serial-to-parallel shift register connected to the clock receiver, the first processing data receiver, and the internal circuit, the clock signal output by the clock receiver clocking the shift register.

20 7. The device of claim 5 wherein the slave circuit further includes a parallel-to-serial shift register connected to the internal circuit, the second multiplexor, and the clock receiver, the shift register outputting a data output signal in response to a parallel data signal from the internal circuit, the clock signal output by the clock receiver clocking the parallel-to-serial shift register.

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8. The device of claim 7 wherein the slave circuit further includes a logic circuit connected to the first mux, the second mux, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

9. The device of claim 8 wherein the media receiver receives a signal from the transmission media having a first frequency, wherein the signal output from the serdes has a second frequency, and wherein the first frequency and the second frequency are substantially equivalent.

10. A processing circuit comprising:
an internal circuit; and
a slave circuit connected to the internal circuit, the slave circuit having:

a clock receiver connectable to a clock driver, the clock receiver outputting a clock signal in response to a millivolt differential signal received from the clock driver;

20 a first processing data receiver connectable to the first physical layer data driver, the first processing data receiver outputting a first signal in response to a millivolt differential signal received from the first physical layer data driver;

25 a first processing data driver connectable to a first physical layer data receiver, the first processing data driver being connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver.

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11. The circuit of claim 10 wherein the slave circuit further comprises:

5 a first multiplexor connected to the clock input receiver and the first processing data receiver, the first multiplexor passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

10 a second multiplexor connected to the first multiplexor and the first communication data driver, the second multiplexor passing a signal output from the first multiplexor when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexor being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 1225 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9230 9235 9240 9245 9250 9255 9260 9265 9270 9275 9280 9285 9290 9295 9300 9305 9310 9315 9320 9325 9330 9335 9340 9345 9350 9355 9360 9365 9370 9375 9380 9385 9390 9395 9400 9405 9410 9415 9420 9425 9430 9435 9440 9445 9450 9455 9460 9465 9470 9475 9480 9485 9490 9495 9500 9505 9510 9515 9520 9525 9530 9535 9540 9545 9550 9555 9560 9565 9570 9575 9580 9585 9590 9595 9600 9605 9610 9615 9620 9625 9630 9635 9640 9645 9650 9655 9660 9665 9670 9675 9680 9685 9690 9695 9700 9705 9710 9715 9720 9725 9730 9735 9740 9745 9750 9755 9760 9765 9770 9775 9780 9785 9790 9795 9800 9805 9810 9815 9820 9825 9830 9835 9840 9845 9850 9855 9860 9865 9870 9875 9880 9885 9890 9895 9900 9905 9910 9915 9920 9925 9930 9935 9940 9945 9950 9955 9960 9965 9970 9975 9980 9985 9990 9995 9999

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14. The circuit of claim 13 wherein the slave circuit further includes a logic circuit connected to the first mux, the second mux, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

15. A physical layer device connectable to a transmission medium, the device comprising:

a media driver connectable to the transmission medium;

10 a media receiver connectable to the transmission medium;
a serializer/deserializer (serdes) connected to the media driver
and the media receiver, the serdes outputting a master clock signal,
an equivalent in-phase slave clock signal when in a calibration mode,
and a data signal when in a data mode, the data signal representing
15 a data signal received from the media receiver; and

a master circuit, the master circuit having:

a clock driver connected to output the master clock signal as a millivolt differential signal;

a first physical layer data driver connectable to output the slave clock signal as a millivolt differential signal when the serdes is in the calibration mode, and the data signal as a millivolt differential signal when the serdes is in the data mode.

16. The device of claim 15 wherein the master circuit further includes:

25 a first physical layer data receiver that receives a signal which
represents the master clock signal during a first phase of the

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calibration mode, and represents the slave clock signal during a second phase of the calibration mode; and

5 an aligner connected to the first physical layer data receiver, the aligner receiving the master clock signal when the first physical layer data receiver receives the master clock signal, and the slave clock signal when the first physical layer data receiver receives the slave clock signal, the aligner having phase comparison circuitry that compares a phase of the master clock signal received by the aligner with a phase of the slave clock signal received by the aligner to 10 determine a phase difference.

17. The device of claim 16 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signals to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the slave clock signal output from the serdes an amount so that the slave clock signal received by the aligner is substantially in phase with the master clock signal received by the aligner when in the calibration mode, the data signal being delayed the amount when in the data mode.

20 18. A method for operating a communication device having a physical layer device connected to a transmission medium and a processing device connected to the physical layer device, the method comprising the steps of:

25 outputting a master clock signal from the physical layer device over a first path;

 receiving the master clock signal in the processing device from the first path;

outputting the master clock signal as a feedback master clock signal from the processing device over a feedback path;

receiving the feedback master clock signal in the physical layer device from the feedback path;

5 determining a phase of the feedback master clock signal;

outputting a slave clock signal from the physical layer device over a second path after the phase of the feedback master clock signal has been determined, the master clock signal and the slave clock signal having an equivalent frequency;

10 receiving the slave clock signal in the processing device from the second path;

outputting the slave clock signal as a feedback slave clock signal from the processing device over the feedback path;

receiving the feedback slave clock signal in the physical layer device from the feedback path;

15 determining a phase of the feedback slave clock signal;

comparing the phase of the feedback master clock signal with the phase of the feedback slave clock signal to determine a phase difference; and

20 adjusting a delay so that the phase of the feedback slave clock signal is substantially aligned with the phase of the feedback master clock signal.

19. The method of claim 18 and further comprising the steps of:

25 outputting a data clock signal from the physical layer device over the first path after the phase difference has been determined;

outputting an input data signal from the physical layer device over the second path after the phase difference has been

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determined, the input data signal and the data clock signal having an equivalent frequency; and

converting the input data signal to a parallel word by clocking the input data signal with the data clock signal.

5 20. A communication device comprising:

a physical layer device connectable to a transmission medium, the device having a master circuit, the master circuit having:

a clock output;

a first data output;

10 a first data input;

a phase comparator connected to the first data input;

and

a processing circuit having a slave circuit, the slave circuit having:

15 a clock input connected to the clock output;

a second data input connected to the first data input;

a second data output connected to the first data input;

and

20 a switch for connecting an output signal from the clock input to the second data output, or an output signal from the second data input to the second data output, the phase comparator comparing a phase of the output signal from the clock input with a phase of the output signal from the second data input to determine a phase difference.